CLASSICAL ELECTRONIC ARCHITECTURES FOR QUANTUM COMPUTERS

PROF. DR.-ING. LOTTE GECK

Member of the Helmholtz Association

JÜLICH Forschungszentrum | Integrated Computing Architectures ICA

ABOUT ME

Junior Professor „System Engineering for Quantum Computing“ at RWTH University (Electrical Engineering Faculty)

QC scientific coordinator at Integrated Computing Architectures (ICA) Institut at Forschungszentrum Jülich

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Other lectures:

Building a Quantum Computer, SS

Quantum Mechanics for Electrical Engineers, WS

ABOUT THE TEAM

- About 30 people
  - 6 Bachelor and Master students
  - 7 PhDs
  - 5 Postdocs
  - 12 Scientists and Engineers

Diverse backgrounds:

- Software Development
- Computer Science
- Physics
- Electrical Engineering

→ especially circuit designers

from academia and industry

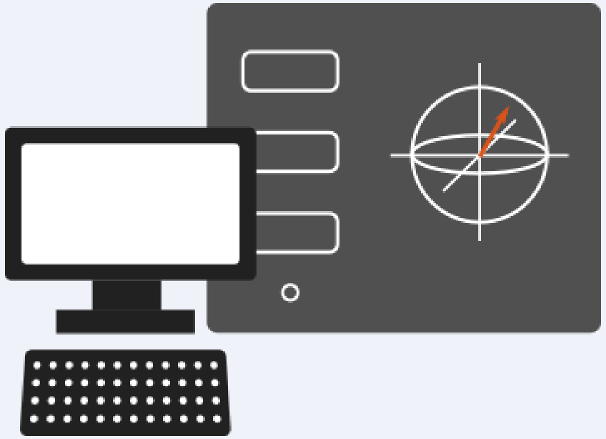
Website

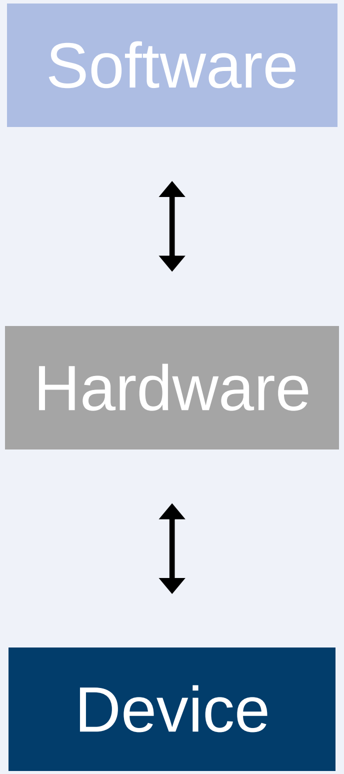
53 qubits?
What if we want or need a million?

Cryostat for Quantum Computing at Google

[1] https://www.wired.co.uk/article/quantum-supremacy-google-microsoft-ibm

What defines a computer?





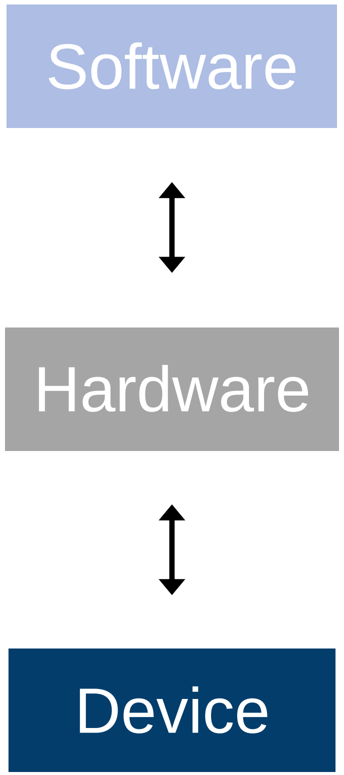
LEVELS OF ABSTRACTION

Dealing with complexity

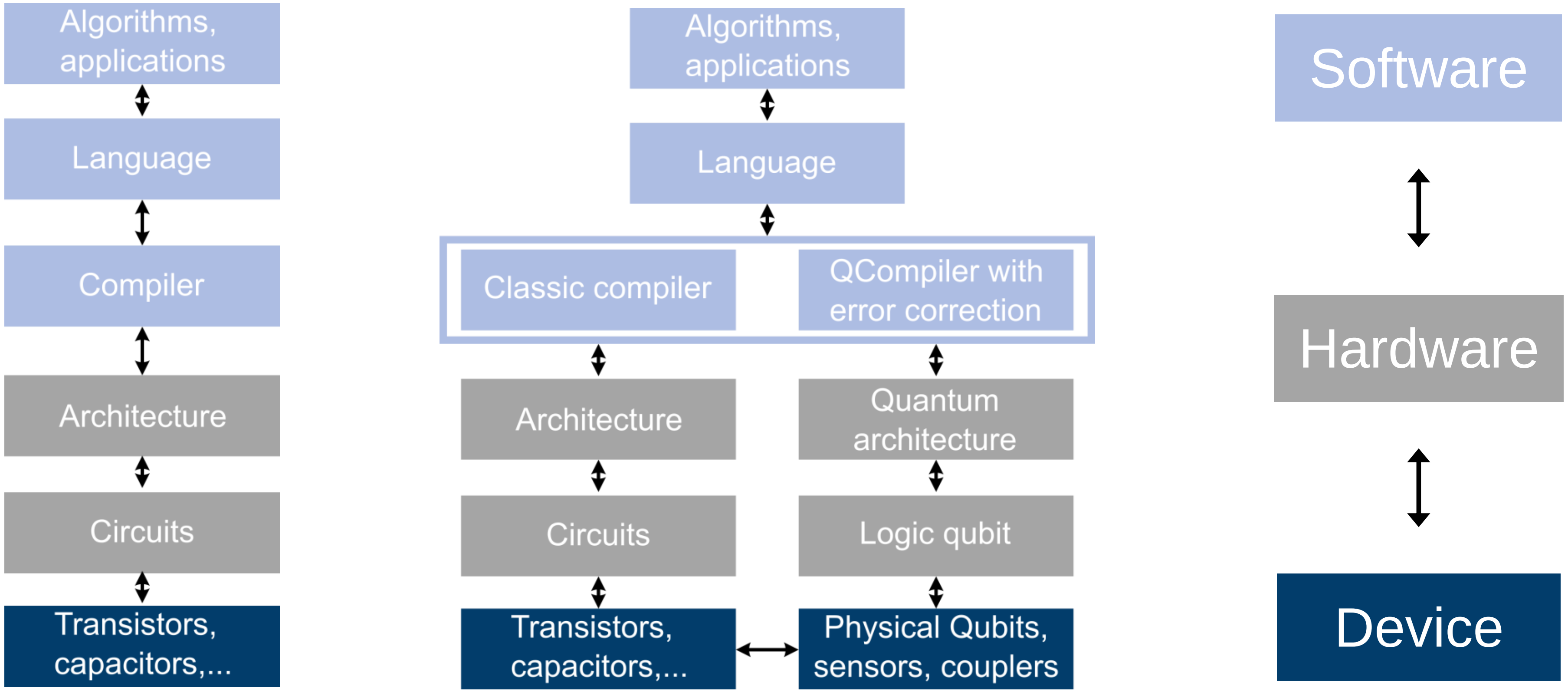
- Hiding complexity where possible
- Layers with different levels of abstraction
- One Layer depends on the layer below to function
- Interfaces and tasks have to be defined

➔ Not every player has to know the whole system

- Famous example: The Internet
  - Based on the Open Systems Interconnect Model (OSI Model)



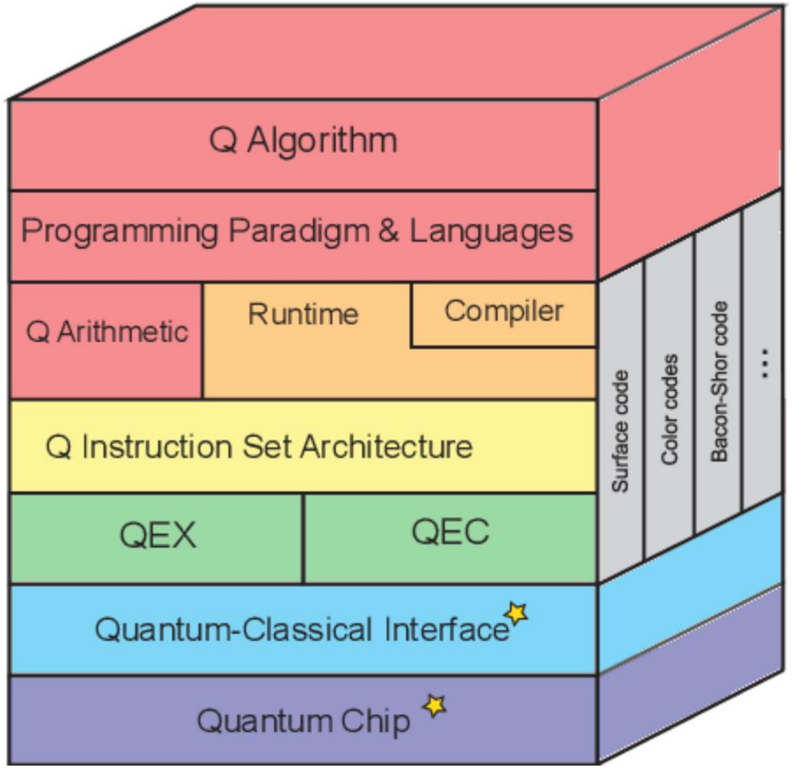
LEVELS OF ABSTRACTION



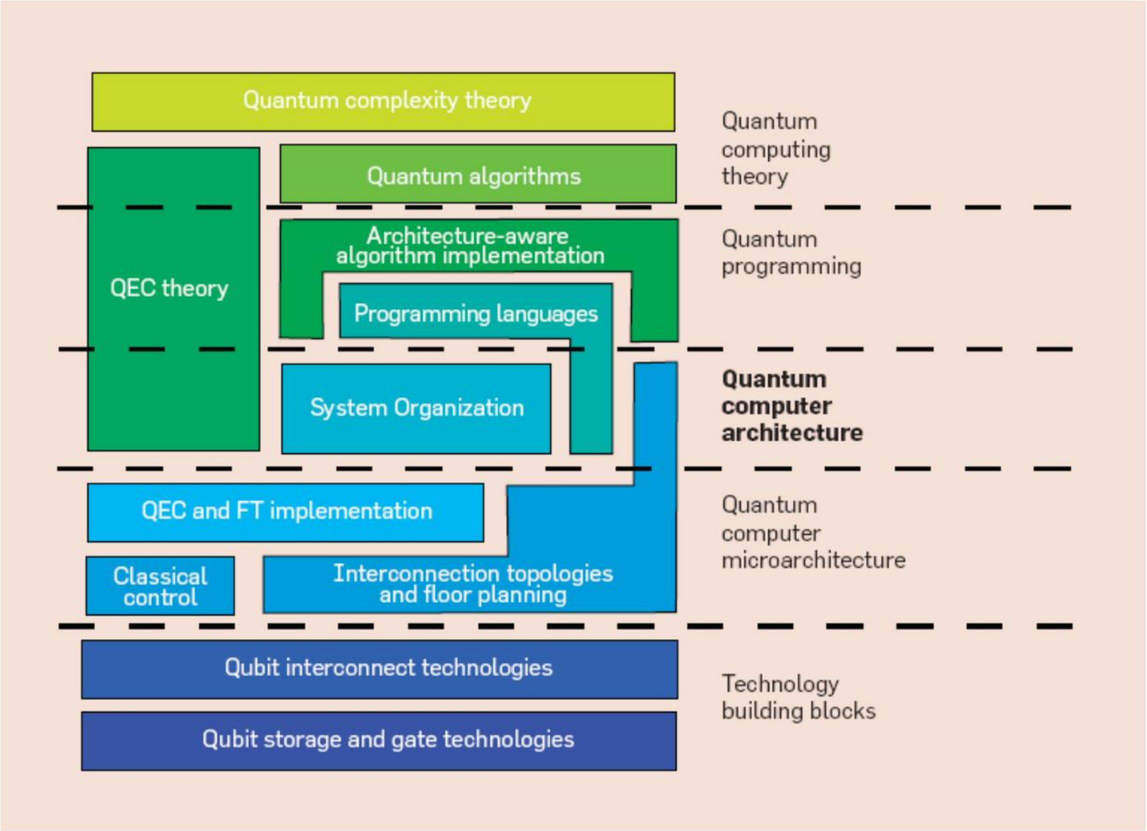
Classical Computer

Quantum Computer

OTHER QUANTUM STACK DEPICTIONS



Fu et al, DOI:10.1145/2903150.2906827

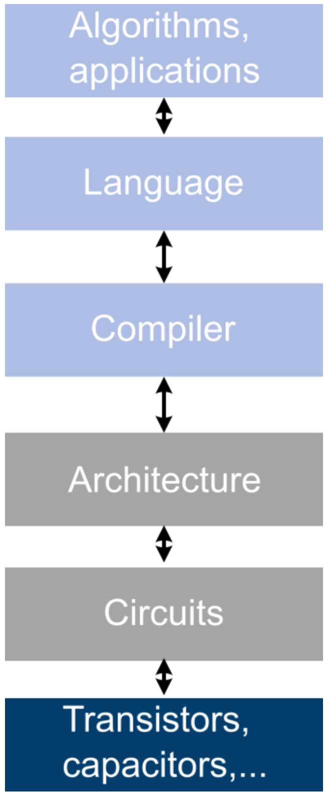


quantumcomputing.stackexchange.com/questions/9067/how-is-a-quantum-computer-programmed

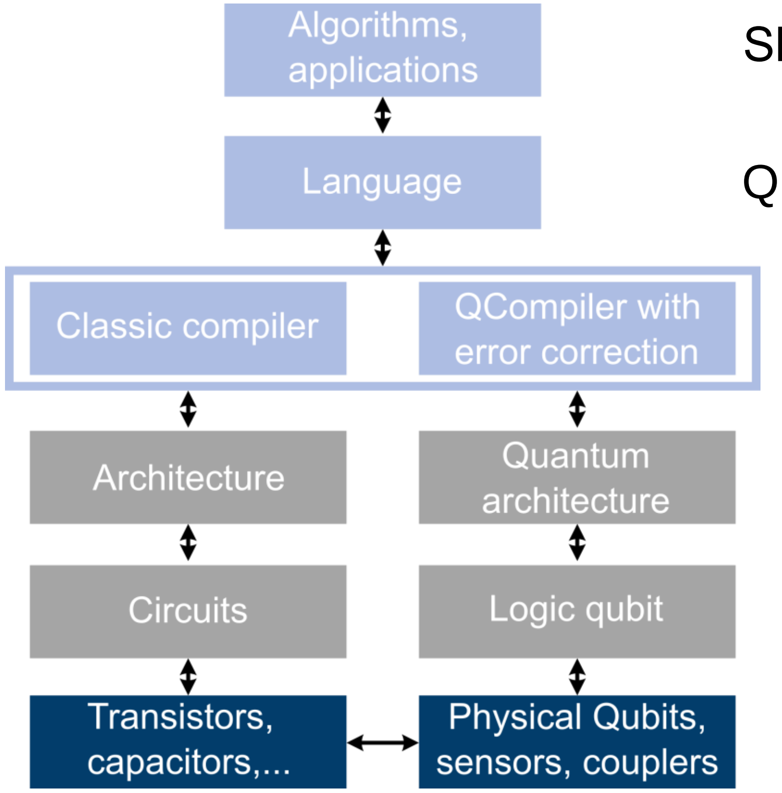
LEVELS OF ABSTRACTION

Numerical optimization,…

C, Python, …



Classical Computer



Quantum Computer

Shor‘s Algorithm, …

Qiskit, Q#, Cirq, …

Language and software development kits (sdks)

LEVELS OF ABSTRACTION

Classic Compiler

- Compiler translates a program in a high-level programming language to binary

```
int main () {
	printf(„Hello World“);
	return 0;
}
```

```
org		0x100
mov		dx, msg
mov		ah, 9
int		0x21
mov		ah, 0x4c
int		0x21
message db 'Hello World!',
0x0d, 0x0a, '$'
```

```
00000000  7f 45 4c 46 01 01 01 00  00 00 00 00 00 00 00 00
00000010  02 00 03 00 01 00 00 00  54 80 04 08 34 00 00 00
00000020  00 00 00 00 00 00 00 00  34 00 20 00 01 00 00 00
00000030  00 00 00 00 01 00 00 00  00 00 00 00 00 80 04 08
00000040  00 80 04 08 74 00 00 00  74 00 00 00 05 00 00 00
00000050  00 10 00 00 b0 04 31 db  43 b9 69 80 04 08 31 d2
00000060  b2 0b cd 80 31 c0 40 cd  80 48 65 6c 6c 6f 20 77
00000070  6f 72 6c 64
00000074
```

High level language

Assembler

Hardware dependent!

Binary code

LEVELS OF ABSTRACTION

Quantum Compiler: the basic idea

Quantum hardware dependent!

Error correction

Code dependent!

Classical hardware dependent!

High level command → Map to logical qubit → Map to physical qubit → Map to binary

```
q_add(a,b,cin)
```

```
CCNOT    ql1, ql2,ql4
CNOT     ql1,ql2
CCNOT    ql2,ql3,ql4
CNOT     ql2,ql3
CNOT     ql1,ql2
```

```
CNOT     q3,q4
H        q1
CNOT     q1,q10
CNOT     q1,q9
CNOT     q1,q12
CNOT     q1,q11
H        q1
Meas     q1
```

```
00 00 00 00 00 00 00 00 34
00 20 00 01 00 00 00 00 00
00 30 00 00 00 00 01 00 00
00 00 00 00 00 00 80 04 08
00 00 00 40 00 80 04 08 74
00 00 00 74
........
```

EXAMPLE: SHOR CODE

Factorizing a L=2048 bit number

d=distance

	Physical Qubits (sum)	
6L logical qubits	12.288	without error correction
8 x to build ancilla factories	98.304	
1.33 x to provide 'wiring' room to move logical qubits	133.000	
10k x for defect form of surface code (d=56)	1.3 bn	
4 x micro-architecture and yield details	>5bn	with error correction

The largest number of qubits in a QC is used for error correction

Idea from EE4575 course, Van Meter et al., Communications of the ACM, 2013

LEVELS OF ABSTRACTION

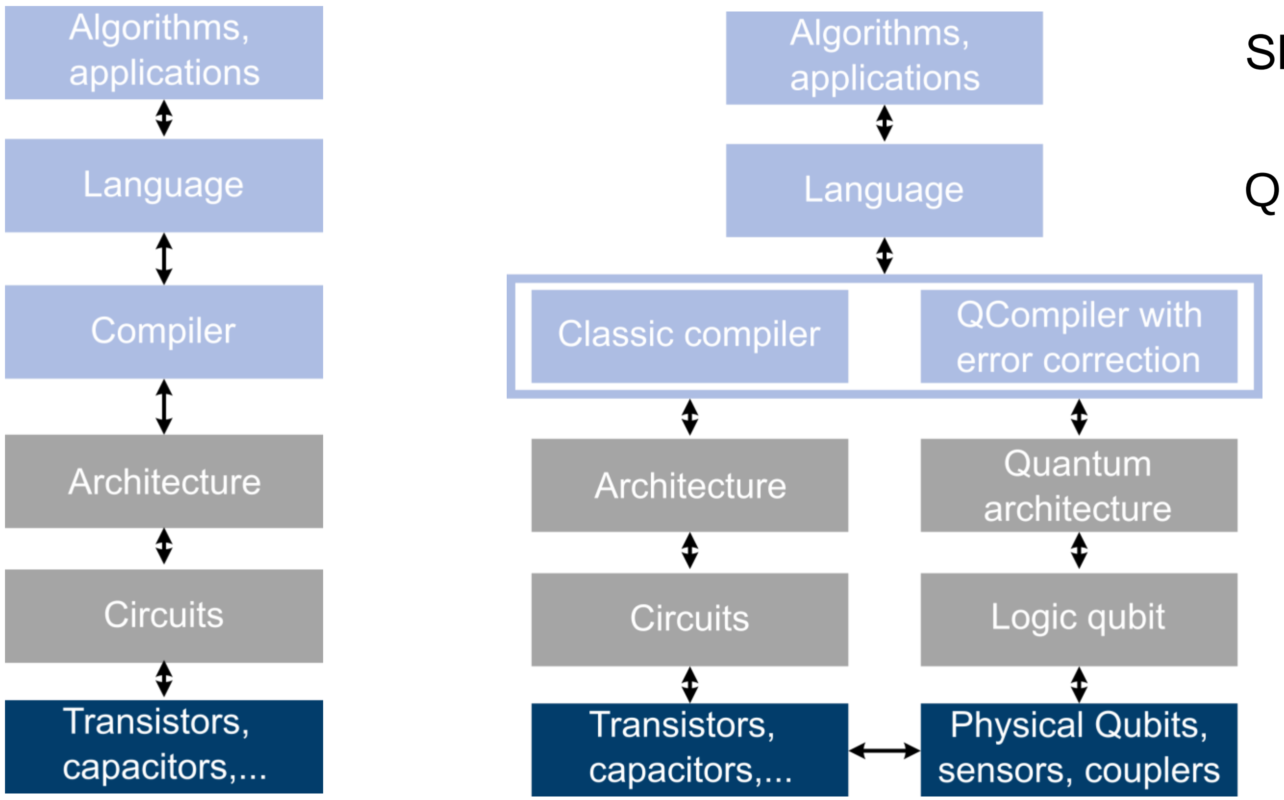
Numerical optimization,…

C, Python, Matlab, …

Shor‘s Algorithm, …

Qiskit, Q#, Cirq, …

Language and software development kits (sdks)

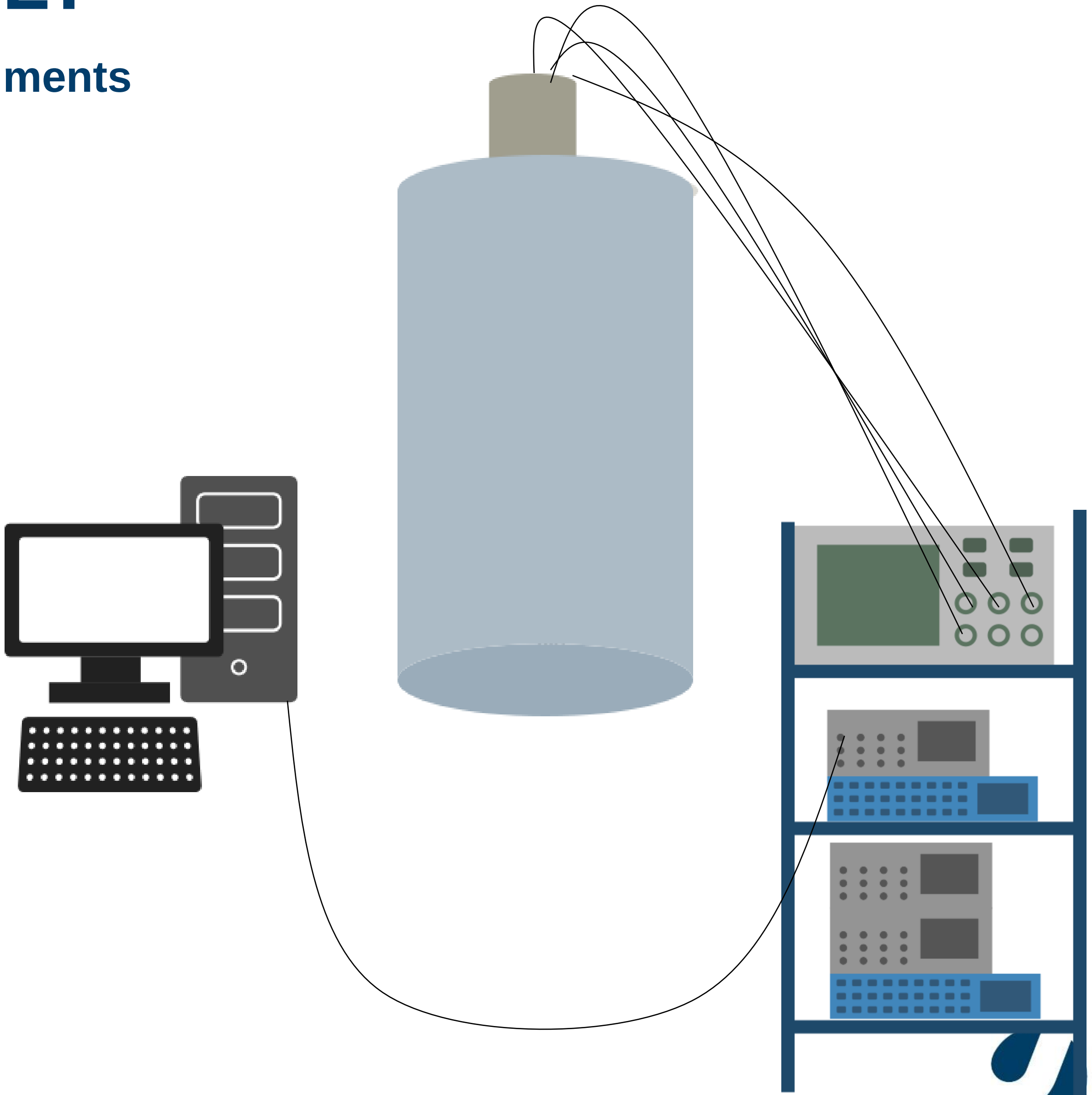


Classical Computer

Quantum Computer

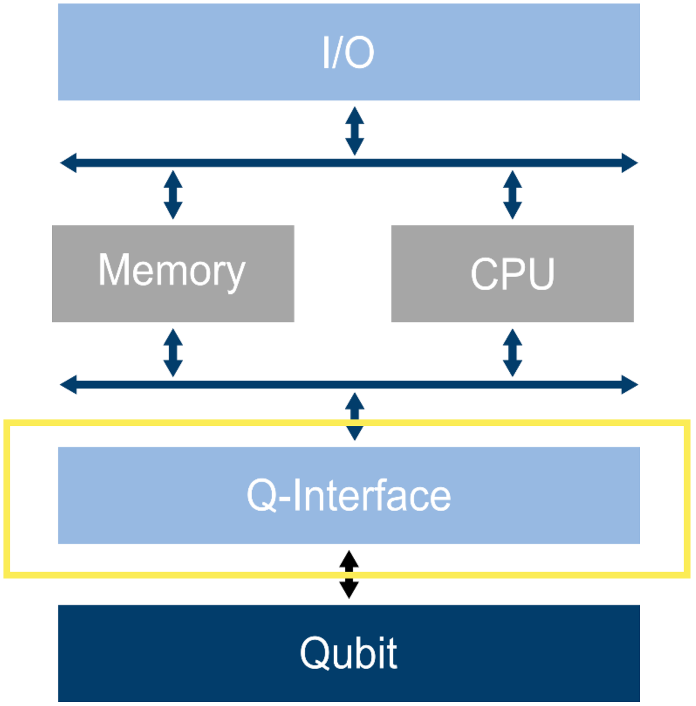
CURRENTLY

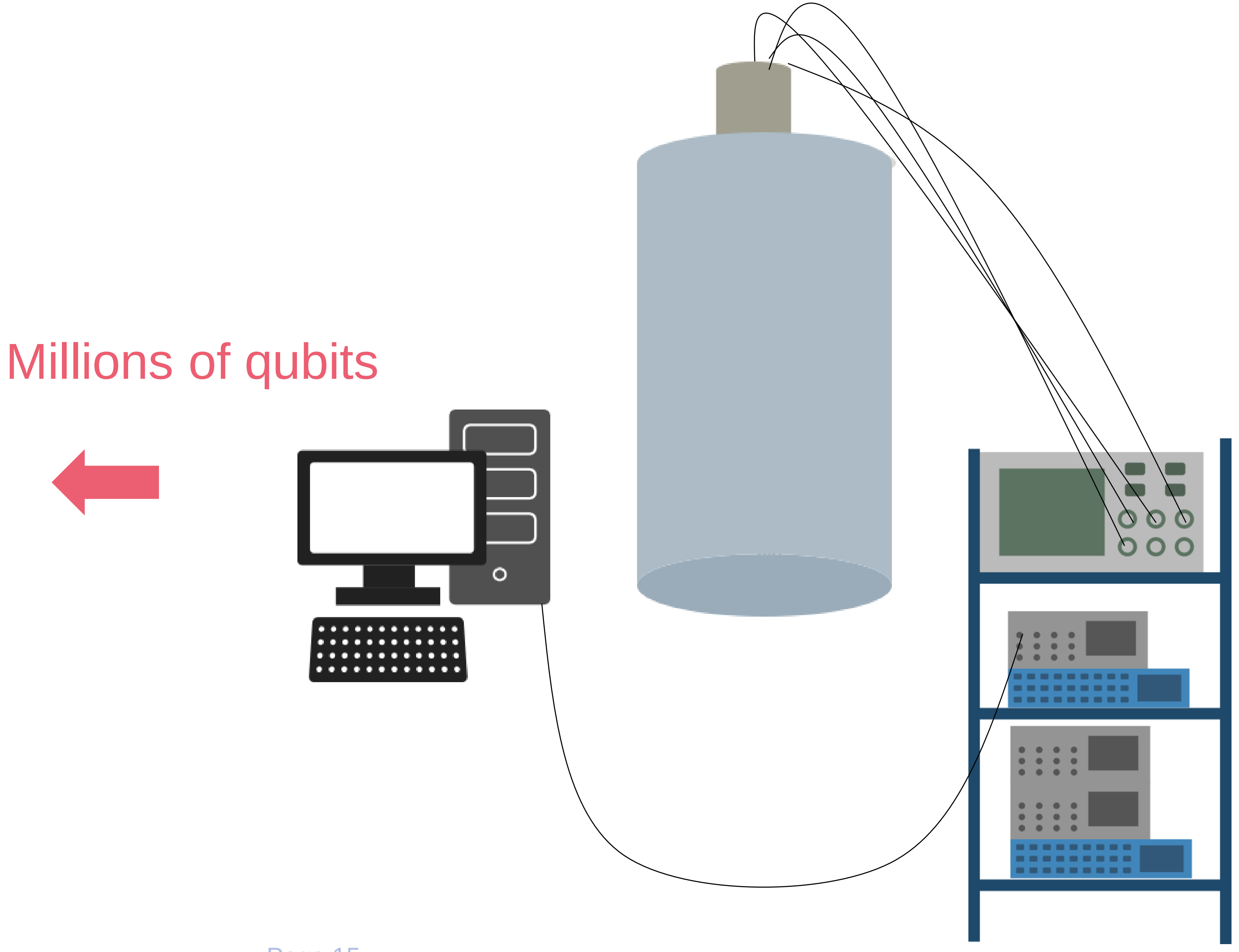
Few Qubits Experiments



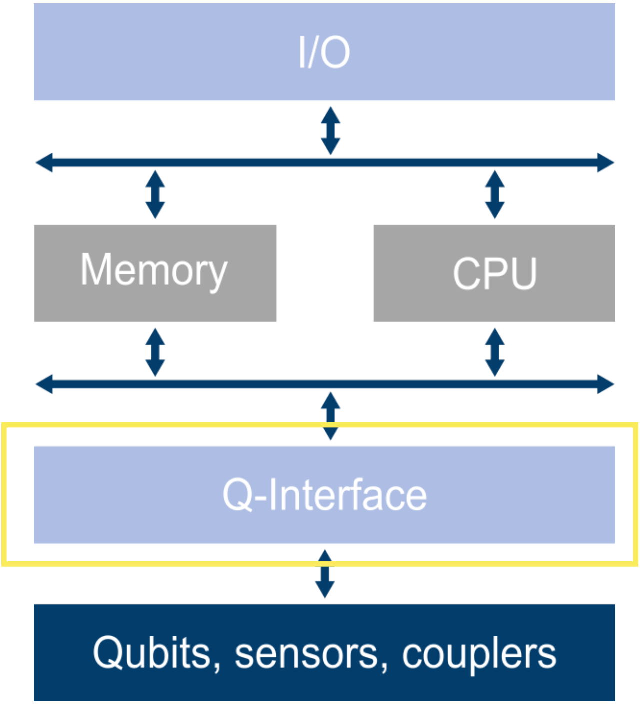
GOAL

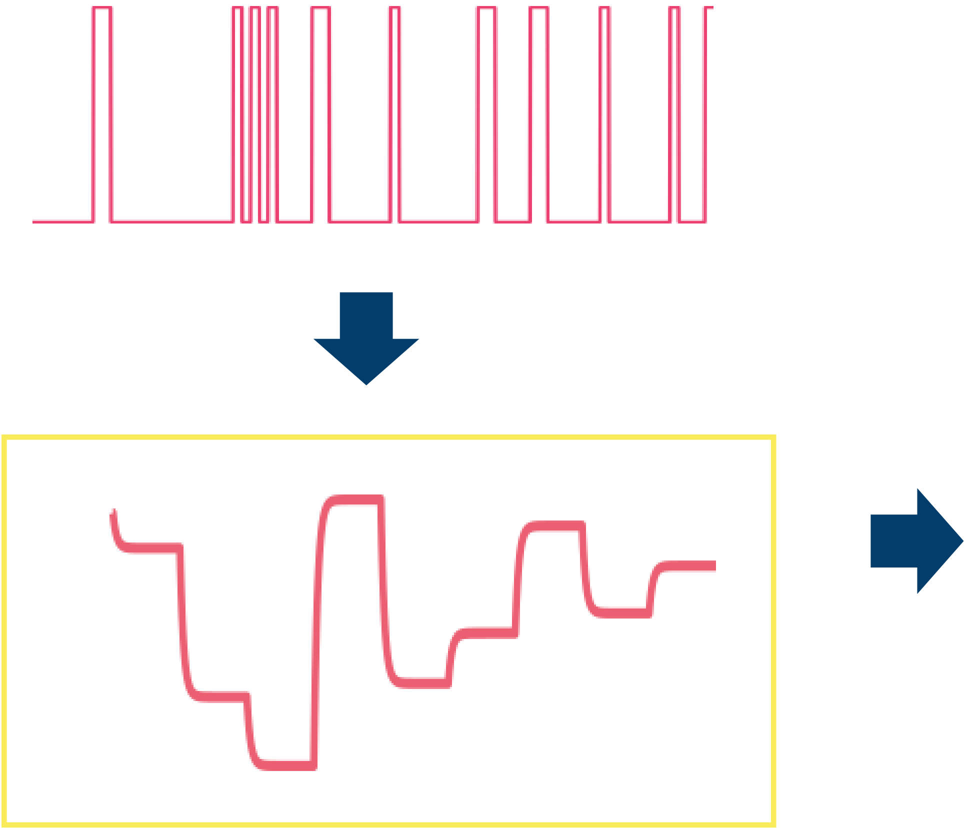
QC as one machine

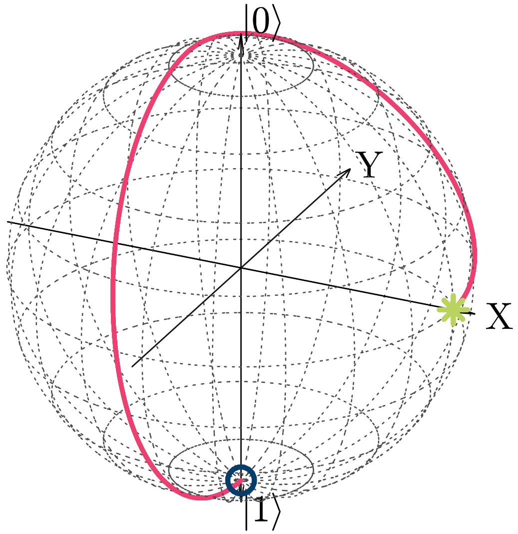




QUANTUM COMPUTER HARDWARE







CHALLENGES QUANTUM INTERFACE

Scalability

- “Moving target”
  - Research on qubits is ongoing → changing requirements
- Performance
  - Qubit states are very fragile → high quality signals
  - Best state-of-the art equipment used
- Wiring bottleneck
  - Several signals/wires per qubit >10^6 wires
  - Not feasible because of size, heat, cost, reliability
- Electronic complexity
  - Control, readout, tuning and error correction
  - Bulky and expensive with off the shelf equipment

Custom integrated circuits near to qubits

At cryogenic temperatures

In current CMOS technology

HOW TO BUILD A QUANTUM COMPUTER

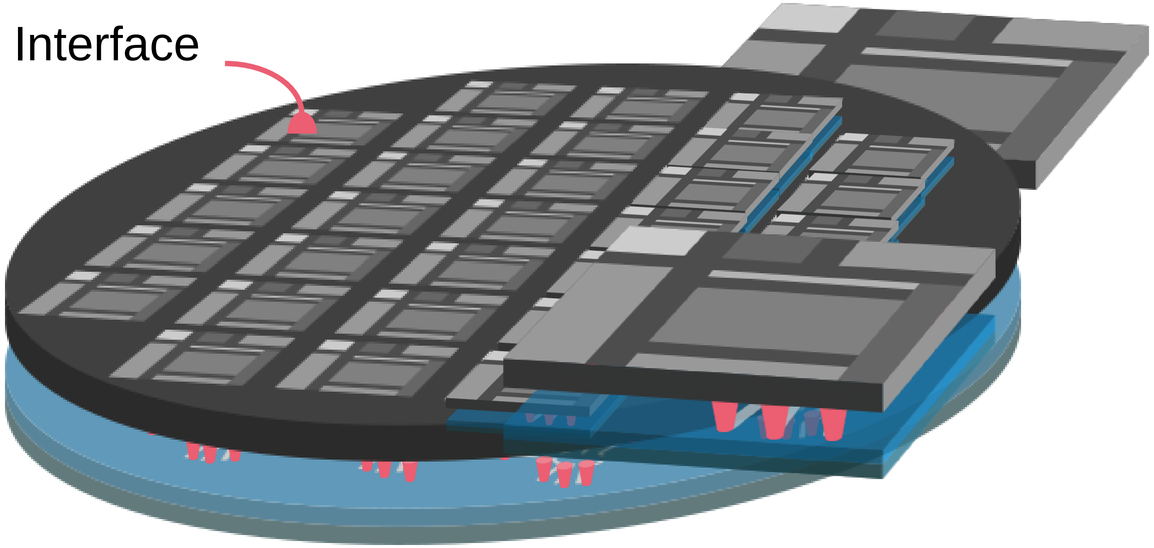
Integrated electronics

Advantages

- Min. inter-temperature connectivity
  - Min. data throughput, cables, heat conduction
- Min. electronics form factor
- Semiconductor industry experience

Disadvantages

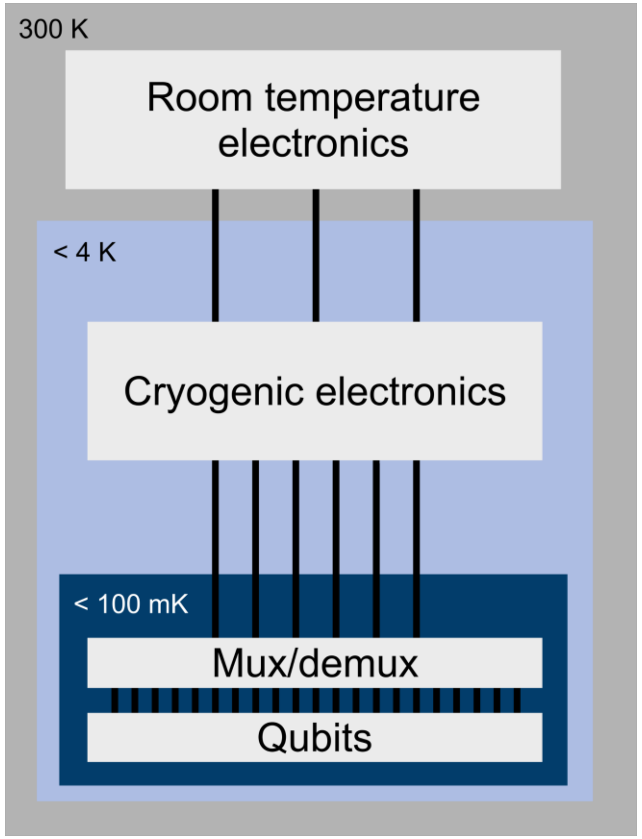
- Restricting area, power limitations
- Cryogenic temperatures not industry standard
  - Sophisticated models not available



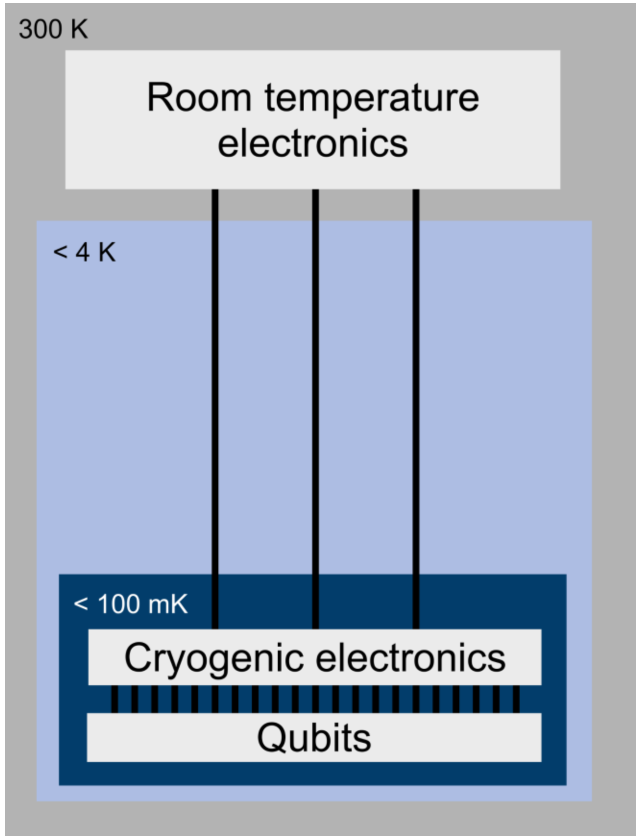
CRYOGENIC OPERATION

- Pure bipolar technology doesn’t work at very low temperatures
- Hetero junction bipolar transistors (HBT) work for some
- Metal-semiconductor FETs (MESFET) work for some
- Potential use of superconducting devices (SQUID, RFSQ,…)
- Advantage:
  - Less thermal noise
- Disadvantage:
  - Outside of industry standard
  - Models and technology not specified

SCALING UP?



300 K
Room temperature electronics
< 4 K
Cryogenic electronics
< 100 mK
Mux/demux
Qubits



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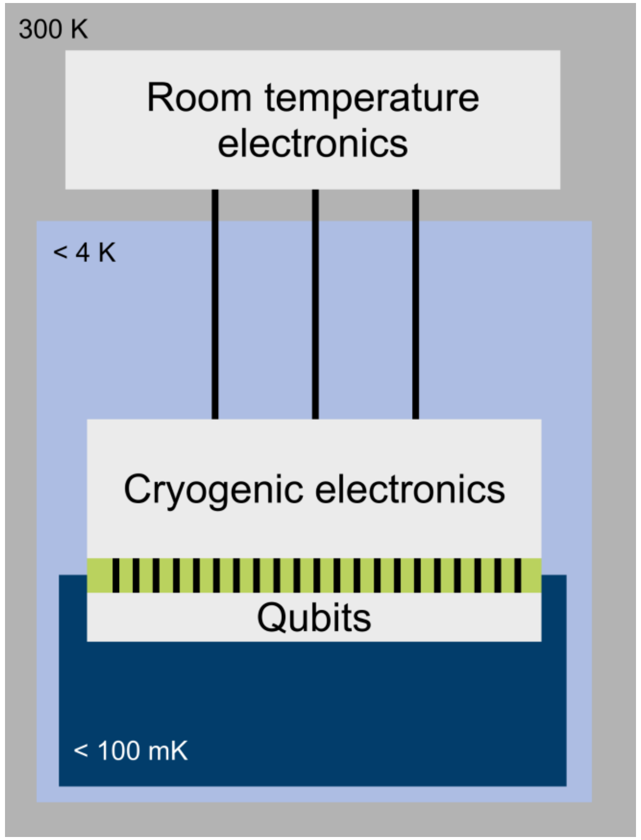
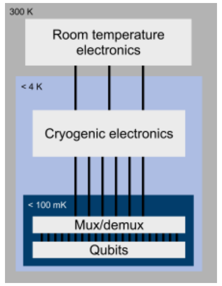
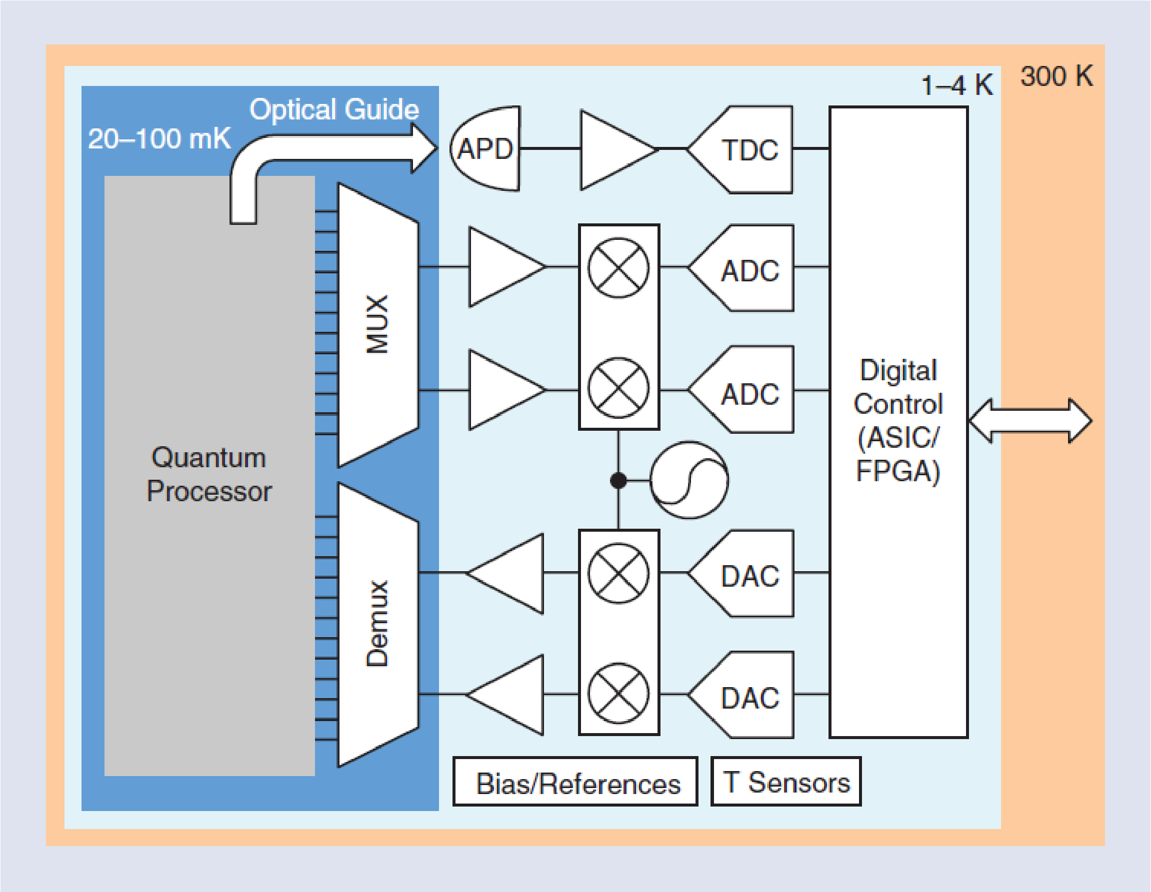


300 K
Room temperature electronics
< 4 K
Cryogenic electronics
Qubits
< 100 mK

INTEGRATED CIRCUITS

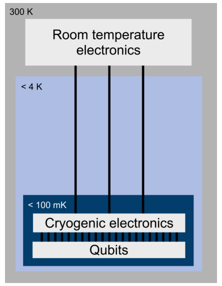


MUX/DEMUX stage example

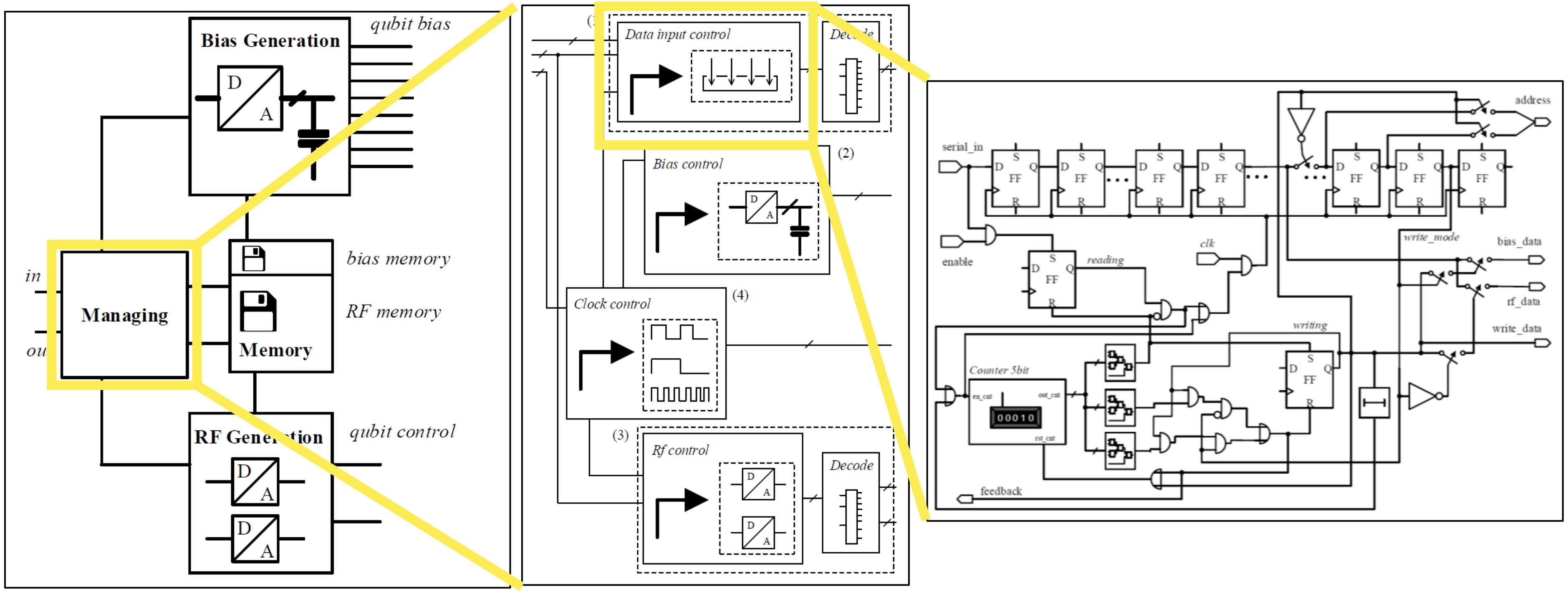


Charbon et al, DOI:10.1109/MMM.2020.3023271

IDEAS FOR MORE SCALABILITY



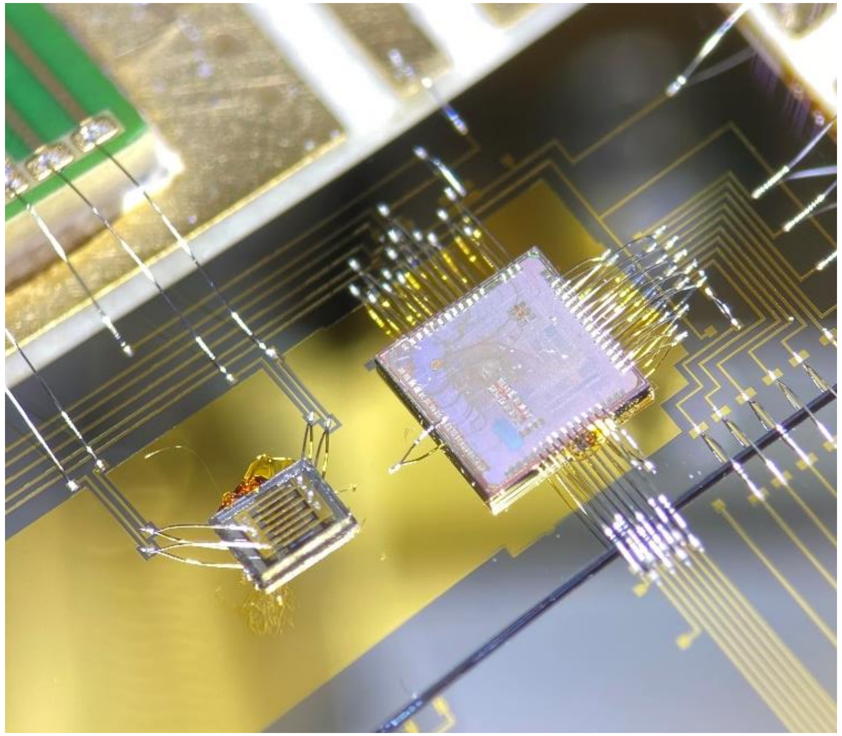
GaAs two spin qubit



L.Geck, ISBN: 978-3-95806-540-6

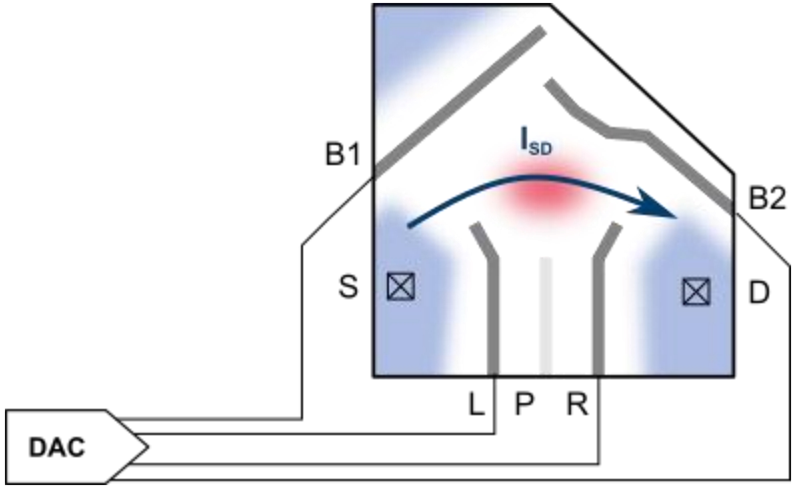
QUANTUM INTERFACE IN PRACTICE

Integrated control chip with qubit

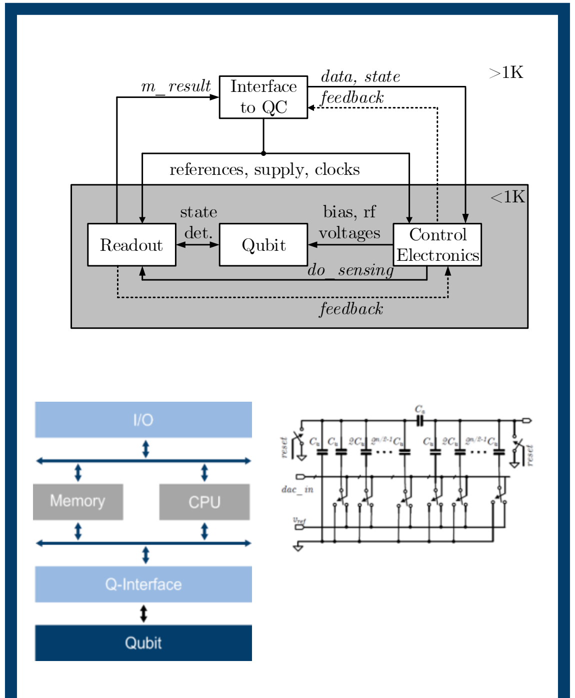


ICA

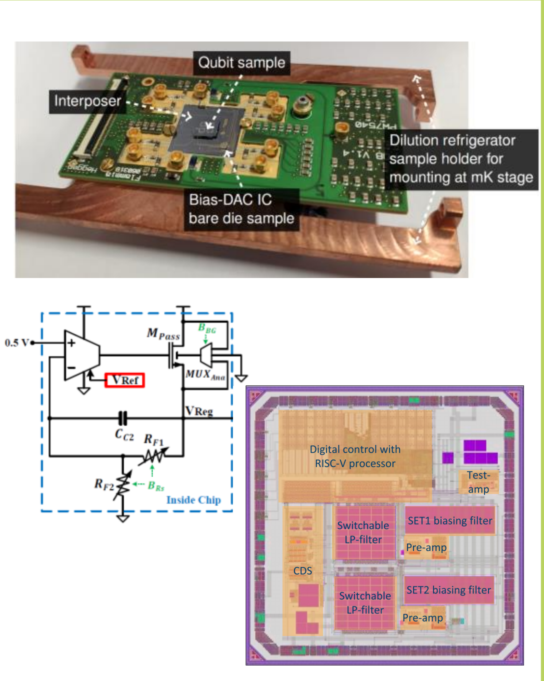
- Control chip and qubit at the same temperature stage in the fridge
- Test GaAs quantum dot as single electron transistor



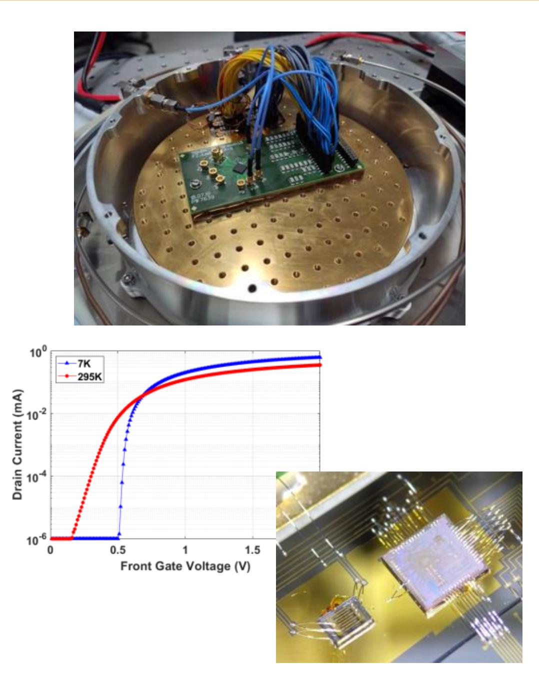
ICA – QC RESEARCH FIELDS



System Modelling
L. Geck



Cryogenic IC Design
P. Vliex



Cryogenic Measurement
C. Degenhardt

System Engineering
M. Schlösser

INTEGRATION WITH CMOS ELECTRONICS

Benefit From Existing Infrastructure To Scale Up

Model, design, implement and test scalable electronic architectures for quantum computers based on cryogenic integrated circuits